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THE COUNTRY CODE AND NUMBER OF YOUR PRIORITY APPLICATION, TO BE USED FOR FILING ABROAD UNDER THE PARIS CONVENTION, IS ***US60/585,632***

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PROVISIONAL APPLICATION FOR PATENT COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c).

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Additional inventors are being named on the 1 *separately numbered sheets attached hereto*

TITLE OF THE INVENTION (500 characters max)

4-BIT ADDER ACCUMULATOR AT 41 GHz CLOCK FREQUENCY IN INP DHBT TECHNOLOGY

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ENCLOSED APPLICATION PARTS ***(check all that apply)***

☑ Specification *Number of Pages* 9

☑ Drawing(s) *Number of Sheets* 4

☐ Application Data Sheet. See 37 CFR 1.76

☐ CD(s), Number

☐ Other (specify)

METHOD OF PAYMENT OF FILING FEES FOR THIS PROVISIONAL APPLICATION FOR PATENT

☐ Applicant claims small entity status. See 37 CFR 1.27.

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FILING FEE Amount ($): 160.00

The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

☐ No.

☑ Yes, the name of the U.S. Government agency and the Government contract number are: Army DAAD17-02-C-0115

Respectfully submitted,

SIGNATURE Daniel J. Long

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Date 7/6/04

REGISTRATION NO. 29,404
(if appropriate)
Docket Number: 20040085 PRO

USE ONLY FOR FILING A PROVISIONAL APPLICATION FOR PATENT

PROVISIONAL APPLICATION COVER SHEET
Additional Page

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[Page 2 of 2]

Number 2 of 2

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EXPRESS MAIL CERTIFICATE EV 509624130 US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Stroili, et al.

Filed: Herein Atty. Dkt. No: 20040085 PRO

For: 4-Bit Adder Accumulator At 41 GHz Clock Frequency In INP DHBT Technology

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CERTIFICATE OF MAILING 37 CFR 1.10: I certify that this correspondence is being deposited on the below date with the U.S. Postal Service with sufficient postage as EXPRESS MAIL addressed to: Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450.

Date: 7-6-04 Gloria Abbasciano

Gloria Abbasciano

Dear Honorable Commissioner:

LETTER OF TRANSMITTAL

Submitted herewith is a Provisional Patent Application consisting of 1 of cover sheet, 9 pages of specification and claims, 4 sheets of drawings.

[X] Invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

DEPOSIT ACCOUNT **190130** AUTHORIZATION – The Office is hereby authorized to charge the required fee, and any deficiency or credit any overpayment in the fees to the above deposit account, owned by BAE SYSTEMS Information and Electronic Systems Integration Inc.

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4-BIT ADDER-ACCUMULATOR AT 41 GHZ CLOCK FREQUENCY IN INP DHBT TECHNOLOGY

Statement of Government Interest

The invention described herein was made under Contract No. DAAD17-02-C-0115 with the Government of the United States of America and may be manufactured and used by and for the Government of the United States of America for Governmental purposes without the payment of any royalties thereon or therefor.

Background of the Invention

1. Field of the Invention

The present invention relates to direct digital synthesizers used in an indium phosphide (InP) heterojunction bipolar transistor (HBT) process. More particularly this invention relates to high speed accumulators for use in such direct digital synthesizers.

2. Brief Description of Prior Developments

High-speed accumulators are frequently used as a benchmark to demonstrate the intrinsic speed and the ability to yield moderately high device count circuits in InP double heterojunction bipolar transistor (DHBT) technology. The accumulator is of particular interest as a building block for direct digital synthesizers (DDS) as is disclosed in] A. Gutierrez-Aitken, J. Matsui, E. N. Kaneshiro, B. K. Oyama, D. Sawdai, A. K. Oki, and D. C. Streit, "Ultrahigh-speed direct digital synthesizer using InP DHBT technology," *IEEE J. Solid-State Circuits*, vol. 37, no. 2, pp. 1115–1119, Sept. 2002. In DDS systems, the frequency range and resolution is determined by the accumulator clock frequency and

data word width. In order to achieve both a high clock frequency and a wide data word width, a combination of modular design and pipelining C. G. Eckroot and S. I. Long, "A GaAs 4-bit adder-accumulator circuit for direct digital synthesis," *IEEE J. Solid-State Circuits*, vol. 23, no. 2, pp. 573–580, Apr. 1988. can be employed in an advanced III-V process.

Summary of Invention

The present invention is a 4-bit, 41 GHz clock frequency accumulator, fabricated in the Vitesse VIP-2 InP DHBT process as is disclosed in G. He, J. Howard, M. Le, P. Partyka, B. Li, G. Kim, R. Hess, R. Bryie, R. Lee, S. Rustomji, J. Pepper, M. Kail, M. Helix, R. Elder, D. Jansen, N. E. Harff, J. Prairie, and E. S. Daniel, "Self-aligned InP DHBT with ft and fmax over 300 GHz in a new manufacturable technology," *IEEE Electron Device Letters*, 2004, submitted for publication, which has ft and fmax both over 300 GHz.

Brief Description of the Drawings

The present invention is further described with reference to the accompanying drawings wherein:

Figure 1 is a schematic drawing showing a 2-bit adder comprised of sum and carry circuits;

Figure 2 is a schematic drawing showing a 4-bit adder-accumulator using pipelined 2-bit adders;

Figure 3 is a schematic drawing showing a single-level parallel-gated carry circuit with cascaded latch;

Figure 4 is a schematic drawing showing a single-level parallel-gated carry circuit with cascaded latch;

Figure 5 is a schematic drawing showing a functional schematic of the accumulator test circuit ;

Figure 6 is a schematic drawing showing a oscilloscope screen capture of the DAC output of 4-bit adder-accumulator test circuit with 41 GHz clock frequency and input increment of 7, with digital sequence labeled on waveform;

Figure 7 is a schematic drawing showing a oscilloscope screen capture of the DAC output of 4-bit adder-accumulator test circuit with 41 GHz clock frequency and input increment of 8 acting as a divide by two circuit with a 20.5 GHz output;

Figure 8 is a schematic drawing showing a oscilloscope screen capture of the carry test circuit output at 27.5 GHz with a 55 GHz clock frequency; and

Figure 9 is a schematic drawing showing a microphotograph of single-level parallel-gated carry test circuit.

Detailed Description of the Preferred Embodiment

A modular 2-bit adder (Fig. 1) forms the basis for the pipelined accumulator (Fig. 2). While a 4-bit accumulator is demonstrated, the 2-bit adder can be cascaded to an arbitrary 2N-bit width. This makes the adder-accumulator particularly useful in DDS applications where the larger bit width allows for greater DDS output resolution. Additionally, the pipelined structure of the adder-accumulator allows for the expansion to wider data words while preserving high clock frequency operation.

In the adder, the 2-bit sum and carry operations are:

$$C_1 = A_0 \cdot B_0 + A_0 \cdot C_0 + B_0 \cdot C_0 \qquad (1)$$

$$C_2 = A_1 \cdot B_1 + A_1 \cdot C_1 + B_1 \cdot C_1 \qquad (2)$$

$$S_0 = A_0 \oplus B_0 \oplus C_0 \qquad (3)$$

$$S_1 = A_1 \oplus B_1 \oplus C_1 \qquad (4)$$

The sum terms are implemented using a 4-level series gated arrangement T. Mathew, S. Jaganathan, D. Scott, S. Krishnan, Y. Wei, M. Urtega, M. Rodwell, and S. Long, "2-bit adder carry and sum logic circuits clocking at 19 GHz clock frequency in transferred substrate HBT technology," in *Proc. IEEE International Conference on Indium Phosphide and Related Materials*, Nara, Japan, May 2001, pp. 505–508, T. Mathew, S. Jaganathan, D. Scott, S. Krishnan, Y. Wei, M. Urtega, M. J. W. Rodwell, and S. Long, "2-bit adder: carry and sum logic circuits at 19 GHz clock frequency in InAlAs/InGaAs HBT technology," *Electronics Letters*, vol. 37, no. 19, pp. 1156–1157, Sept. 2001. By merging the combinational logic functions with the latch operation, propagation delay is reduced. This allows for higher-speed operation at the expense of a larger supply voltage. The carry terms are implemented using a single-level parallel-gated logic structure with a cascaded latch (Fig. 3). This allows for a lower supply voltage than 4- level series-gated logic, while still operating at high clock frequencies.

The use of single-level parallel-gated logic is well suited for the carry terms since the carry operation essentially detects when two or three of the inputs are high. When all three of the inputs are either high or low, a full differential is seen across Xp and Xn, since all of the current is steered through one leg of the circuit. When one or two of the inputs are high, the differential across Xp and Xn is reduced, since 1/3 of the current is

steered through one leg of the circuit while 2/3 of the current is steered through the other leg of the circuit (Fig. 4). Although this method has a reduced differential for some input states, the differential across Xp and Xn is sampled by the latch which generates a full differential for propagation to subsequent stages. The single-level parallel-gated carry circuit potentially pro-vides a mechanism for overall power reduction. Currently, the sum circuit constrains the power supply from being lowered to take advantage of the carry design, since the sum circuit is a 4-level series gated design. In computer simulations with an alternative sum circuit using fewer voltage levels, one diode drop is removed from the supply voltage resulting in approximately 15% reduction in power.

II. TEST CIRCUITS

The adder-accumulator test circuit (Fig. 5) contains a 4-bit adder configured as an accumulator, followed by a 4-bit digital to analog converter (DAC). The design allows for any 4-bit increment (0 through 15) to be input into the accumulator. Since the accumulator has four high-frequency outputs, the on-chip 4-bit DAC is used to generate the test chip output. The DAC output preserves all of the information for determining proper operation in a single high frequency analog output, which can be observed on a sampling oscilloscope. Also demonstrated is a carry test circuit. This circuit is configured with a logic high on the 'A' input, a logic low on the 'B' input, and with the carry output inverted and fed back into the 'C' input. Since the 'A' input is high and the 'B' input is low, the carry circuit tracks the 'C' input. The inversion of the carry output into the 'C' input results in a divide by two circuit.

III. MEASUREMENT RESULTS

The test circuits were tested on wafer using a probe station and high-frequency probes. The output waveforms were measured with a high-frequency sampling oscilloscope.

Two examples of adder-accumulator output sequences are shown. In the first example, an input increment of 7 is used the create the digital sequence of 15, 6, 13, 4, . . In this configuration, the 16 discrete DAC output voltage levels are clearly illustrated (Fig. 6), while operating with a clock frequency of 41 GHz. In the second example, the adder-accumulator is configured as a divide by two circuit (Fig. 7). By using an input increment of 8, the most significant bit of the 4-bit digital value changes every clock cycle, creating a 20.5 GHz output signal from a 41 GHz clock frequency. The carry test circuit yielded a maximum output frequency of 27.5 GHz with a clock frequency of 55 GHz (Fig. 8).

IV. CONCLUSION

We realized a 4-bit adder-accumulator test circuit in InP DHBT technology with a maximum clock frequency of 41 GHz. We also realized a carry test circuit (Fig. 9) with Fig. 9. Microphotograph of single-level parallel-gated carry test circuit. Fig. 10. Microphotograph of 4-bit adder-accumulator test circuit. 150 transistors operating at a maximum frequency of 55 GHz. The adder-accumulator test circuit has 624 transistors in an area of 1725 ¹m by 1025 ¹m (Fig. 10). Overall, the adder-accumulator test circuit consumes 4.1 W of power, while a single 2-bit adder structure is estimated to consume 0.9 W.

The adder-accumulator is modular and pipelined, allowing for expansion to wider data words, while preserving high clock frequency operation. The adder-accumulator also employs a single-level parallel-gated carry circuit. This allows for operation at high clock frequencies while taking a step towards reduced power consumption.

While the present invention has been described in connection with the preferred embodiments of the various figures, it is to be understood that other similar embodiments may be used or modifications and additions may be made to the described embodiment for performing the same function of the present invention without deviating therefrom. Therefore, the present invention should not be limited to any single embodiment, but rather construed in breadth and scope in accordance with the recitation of the appended claims.

Claims

What is claimed is:

1. A method for operating a high-speed 4-bit accumulator in an indium phosphide (InP) heterojunction bipolar transistor (HBT) process, wherein the improvement comprises using 624 transistors while maintaining a 41 GHz operating frequency, whereby high clock rates are obtained by combining the logic functions into pipelined latches.

Abstract

A 41 GHz 4-bit adder-accumulator test circuit implemented in InP double heterojunction bipolar transistor (DHBT) technology using 624 transistors is disclosed. High clock rates are obtained by combining the logic functions into pipelined latches. The adder-accumulator contains a single-level parallel-gated carry circuit that is used as a step towards reduced power consumption. The carry circuit has a maximum clock frequency of 55 GHz. The accumulator architecture employs modular, pipelined 2-bit adders and is cascadable to 2N-bits. The test circuit includes a 4-bit digital to analog converter (DAC) that facilitates demonstration of high-speed operation.

Drawings

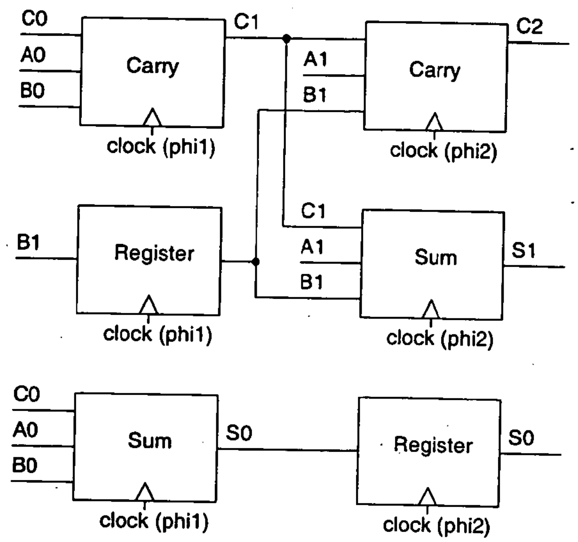

Figure 1

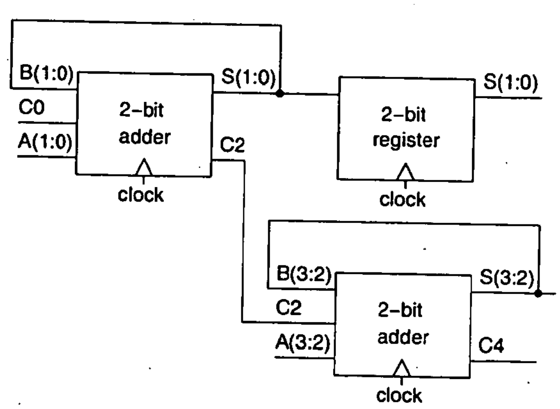

Figure 2

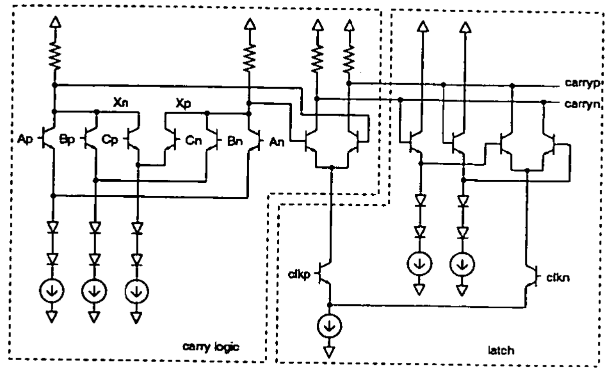

Figure 3

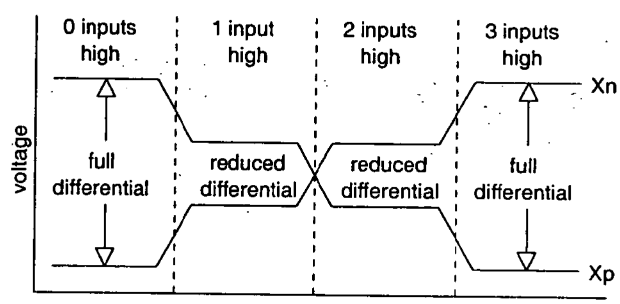

Figure 4

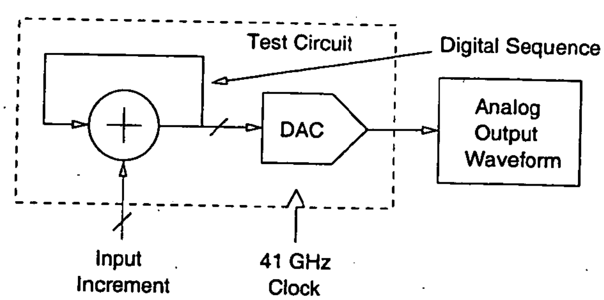

Figure 5

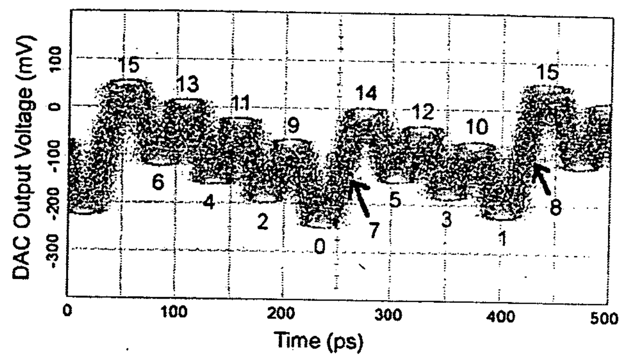

Figure 6

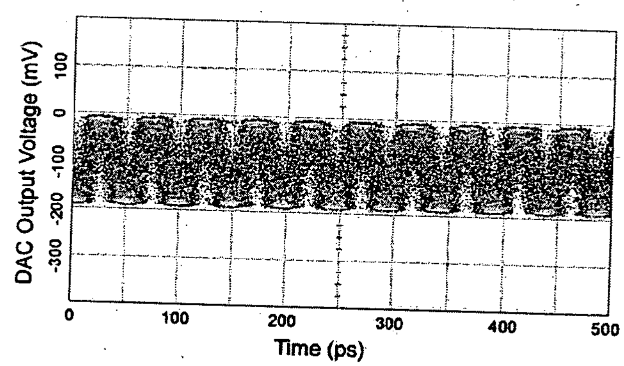

Figure 7

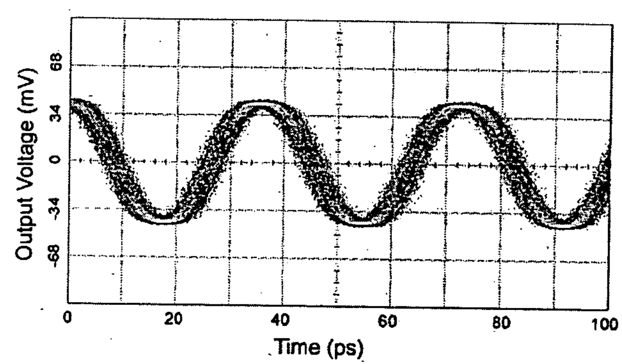

Figure 8

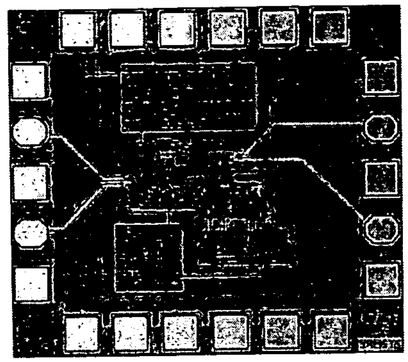

Figure 9